

## Abstract

A memory integrated circuit having three layers of metallic traces disposed over a substrate assembly including various active devices. The traces are arranged to include I/O traces that are continuous in the third layer across spans of 4 or 8 memory blocks of an array, and that are interspersed on the third layer with non-I/O lines adapted to reduce interference between I/O lines. Column select lines, orthogonal to I/O lines and disposed in the third layer of metallic traces, except in the vicinity of I/O lines, are provided in a linear configuration and shielded from parallel digit lines in the first layer of traces by traces of the intervening second layer of traces. Global bleeder lines disposed in the third layer of traces are adapted to apply a standby voltage to a plurality of sense amplifiers. Other features of the invention include two layer power and ground bus traces, and row decoder and phase driver circuits disposed in throat and gap cell regions respectively.